IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:		TI-36952
	Hang-Dony Kuan, et al.	Art Unit: 2829
Serial No:	10/804,374	Examiner: Arleen M. Vazqiez
Filed:	March 19, 2004	Conf. No.: 7211
For:	IC Testing Apparatus and Methods	

Appeal Brief Under 37 C.F.R. §41.37

Board of Patent Appeals and Interferences
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This is Appellant's Appeal Brief filed pursuant to 37 C.F.R. §41.37 in connection with the above-identified application in response to the Final Rejection mailed June 14, 2007, and the Notice of Appeal mailed by Applicant on September 21, 2007.

Real Party in Interest

The real party in interest in this application is Texas Instruments Incorporated, a corporation of Delaware with its principle place of business in Dallas, Texas. An assignment to Texas Instruments Incorporated is recorded at reel 013275 and frame 0196 to 0198.

Related Appeals and Interferences

There are no appeals of interferences related to this appeal in this application.

Status of the Claims

Claims 6-8 and 12-14 are the subject of this appeal. Claims 1-5, 9, and 15-16 are withdrawn. Claims 6-8 and 12-14 are rejected. Claims 10, 11, and 17-19 are cancelled. This application was filed on March 19, 2004.

Status of Amendments Filed After Final Rejection

The Appellants filed an amendment under 37 C.F.R. § 1.116 on August 22, 2007 in response to the Office Action dated June 14, 2007, and the amendment was entered.

Summary of Claimed Subject Matter

Specification page 7, line 9 to page 8, line 9, provides a concise explanation of the invention defined in independent claim 6.

The socket in claim 6 is socket 12 in Figure 2.

The pins in claim 6 are represented by pin 24 in Figure 2.

The device under test in claim 6 is DUT 10 in Figure 2.

The test board in claim 6 is test board 16 in Figure 2.

The pin receptacles in claim 6 are represented by pin receptacle 38 in Figure 2.

The "measuring means" in claim 6 is disclosed in the specification on page 8, lines 7-9. The contact area 36 of the test board 16 is connected to the automatic test equipment (ATE) for making test measurements.

The DUT 10, shown in Figure 1, is mounted in a socket 12. The socket 12 is positioned on a PCB test board 16 designed to interface with automatic test equipment (ATE) 18. Referring to Figure 2, a close-up partial cross-section is shown. The DUT 10 has a contact surface 20, in this case a bond pad 20 with a solder ball 22 attached. A test probe, in this instance a pogo pin 24, extends from the upper surface 26 of the socket 12 to the lower surface 28. The pin 24 functions as an electrical path between the DUT 10 and the test board 16. As shown, the upper tip 30 of the pin 24 contacts the solder ball 22.

At the opposing end 32 of the pin 24, contact 34 is made with a contact area 36 on the test board 16. The contact area 36 has a probe or pin receptacle 38 for receiving the bottom tip 32 of the pin 24 in order to ensure staunch electrical contact 34 between the pin 24 and the contact area 36 on the test board 16. The total area of contact 34 is increased by the correspondence of the pin tip 32 and the pin receptacle 38. The contact area 36 of the test board 16 is connected to the ATE (not shown) for making test measurements as is common in the arts. The electrical path between the DUT 10 and the ATE includes the staunch contact 34 between the pin 24 and pin receptacle 38 through which accurate measurements may be made.

Specification page 7, line 9 to page 8, line 9, provides a concise explanation of the invention defined in independent claim 12.

The socket in claim 12 is socket 12 in Figure 2.

The device under test in claim 12 is DUT 10 in Figure 2.

The contact area in claim 12 is contact area 36 in Figure 2.

The pin in claim 12 is pin 24 in Figure 2.

The pin receptacle in claim 12 is pin receptacle 38 in Figure 2.

The DUT 10, shown in Figure 1, is mounted in a socket 12. The socket 12 is positioned on a PCB test board 16 designed to interface with automatic test equipment (ATE) 18. Referring to Figure 2, a close-up partial cross-section is shown. The DUT 10 has a contact surface 20, in this case a bond pad 20 with a solder ball 22 attached. A test probe, in this instance a pogo pin 24, extends from the upper surface 26 of the socket 12 to the lower surface 28. The pin 24 functions as an electrical path between the DUT 10 and the test board 16. As shown, the upper tip 30 of the pin 24 contacts the solder ball 22.

At the opposing end 32 of the pin 24, contact 34 is made with a contact area 36 on the test board 16. The contact area 36 has a probe or pin receptacle 38 for receiving the bottom tip 32 of the pin 24 in order to ensure staunch electrical contact 34 between the pin 24 and the contact area 36 on the test board 16. The total area of contact 34 is increased by the correspondence of the pin tip 32 and the pin receptacle 38. The contact area 36 of the test board 16 is connected to the ATE (not shown) for making test measurements as is common in the arts. The electrical path between the DUT 10 and the ATE includes the staunch contact 34 between the pin 24 and pin receptacle 38 through which accurate measurements may be made.

Grounds for Rejection to be Reviewed on Appeal

Whether claims 6-8 and 12-14 are unpatentable under 35 USC 102(b) over U.S. Patent No. 6,400,169.

Whether claims 6-8 and 12-14 are unpatentable under 35 USC 102(b) over U.S. Patent No. 5,955,888.

Arguments

Rejection under 35 USC 102(b) as being unpatentable over U.S. Patent No. 6,400,169

Claims 6-8 and 12-14

Claim 6 includes "...a socket for receiving a DUT, the socket having pins with ends for making electrical contact with the DUT and opposing ends for making contact with a test board; the test board adjoining the socket, the test board having pin receptacles for receiving the opposing ends of the pins ...". Claim 12 includes "... a pin receptacle on the contact area for receiving a pin, for thereby making staunch electrical contact between the pin and contact point." The references of record do not show, teach, or suggest the above limitations of claims 6 and 12. U.S. Patent No. 6,400,169 does not show pin receptacles in the test board. 106 in U.S. Patent No. 6,400,169 does not disclose a pin receptacle. U.S. Patent No. 6,400,169, in Figure 7B, only shows a line going across the bottom of Figure 7B at 106. U.S. Patent No. 6,400,169 does not show, teach, or suggest a pin receptacle receiving the opposing end of a pin.

Rejection under 35 USC 102(b) as being unpatentable over U.S. Patent No. 5,955,888

Claims 6-8 and 12-14

Claim 6 includes "...a socket for receiving a DUT, the socket having pins with ends for making electrical contact with the DUT and opposing ends for making contact with a test board; the test board adjoining the socket, the test board having pin receptacles for receiving the opposing ends of the pins ...". Claim 12 includes "... a pin receptacle on the contact area for receiving a pin, for thereby making staunch electrical contact between the pin and contact point." The references of record do not show, teach, or suggest the above limitations of claims 6 and 12. U.S. Patent No. 5,955,888 does not show pin receptacles in the test board. 618 in U.S. Patent No. 5,955,888 is not a pin receptacle, it is solder (column 6, line 38). U.S. Patent No. 5,955,888 does not disclose a "socket having pins with ends for making electrical contact with the DUT

and opposing ends for making contact with a test board". U.S. Patent No. 5,955,888 also does not disclose a "test board having pin receptacles for receiving the opposing ends of the pins". U.S. Patent No. 5,955,888 discloses a pogo pin permanently attached to a printed circuit board 610, not a socket having pins with ends for making electrical contact with the DUT and opposing ends for making contact with a test board. (See Col. 6, lines 31-39)

CONCLUSION

For the foregoing reasons, Appellants respectfully submit that the Examiner's final rejection of Claims 6-8 and 12-14 is improper, and it is respectfully requested that the Board of Patent Appeals and Interferences so find and reverse the Examiner's rejection.

Please charge any fees in connection with the filing of this paper to the Deposit Account No. 20-0668 of Texas Instruments Inc.

Should the Examiner have further inquiry concerning these matters, please contact the below named attorney for Applicant.

Respectfully submitted,

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CLAIMS APPENDIX

6. A system for testing a singulated semiconductor device (DUT) comprising:

a socket for receiving a DUT, the socket having pins with ends for making electrical contact with the DUT and opposing ends for making contact with a test board;

the test board adjoining the socket, the test board having pin receptacles for receiving the opposing ends of the pins; and

measuring means operably coupled to the test board pin receptacles for measuring electrical signals in the DUT.

7. A system according to claim 6 wherein the receptacles each further comprise a basin for receiving the pin.

8. A system according to claim 6 wherein the receptacles each further comprise a generally conical basin for receiving the pin.

12. A test board for use in association with semiconductor device automatic test equipment (ATE) and a socket, the socket having pins and adapted for receiving a device under test (DUT), the test board comprising:

a contact area for operably coupling a pin to the ATE;

a pin receptacle on the contact area for receiving a pin, for thereby making staunch electrical contact between the pin and contact point.

13. A test board according to claim 12 wherein the pin receptacle further comprises a basin for receiving the pin.

14. A test board according to claim 12 wherein the pin receptacle further comprises a generally conical basin for receiving the pin.

EVIDENCE APPENDIX

None

RELATED PROCEEDINGS APPENDIX

None